

REMARKS

This application has been carefully considered in connection with the Office Action dated November 7, 2002. Claims 1-9 are pending. Claims 1-5 have been amended by this response. Reconsideration and allowance is respectfully requested in light of the foregoing amendments and the following remarks.

The Examiner states that Claims 7-9 are allowable over the prior art of record, for which Applicants thank the Examiner. Claims 3-6 stand rejected under 35 U.S.C § 112, second paragraph, as allegedly being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicants regard as their invention. An indication is given that Claims 3-6 would be allowable if rewritten or amended to overcome the rejections under 35 U.S.C. § 112, second paragraph.

Claim 3 has been rejected under 35 U.S.C. § 112, second paragraph. The Examiner states that in Claim 3, "the recitation of 'a pulse width modulated drive signal from the output of the turn on delay circuit' is indefinite because it is unclear as to if this pulse width modulated drive signal is the same as or is an additional signal to the output voltage of the turn on delay circuit recited in line 6." (Office Action, page 2.) Applicants have therefore amended Claim 3 to recite "applying one of the pair of first pulse width modulated signals to a set input of a latch...", "applying the other of the pair of first pulse width modulated signals...", and "obtaining a second pulse width modulated drive signal from the output of the turn-on delay circuit." Also, for purpose of clarity, Applicants have deleted the parenthetical term "(symmetrical)" for Claim 3.

Applicants respectfully submit that the foregoing amendment overcomes the rejection of the Examiner, and respectfully request that the 35 U.S.C. § 112, second paragraph, rejection be withdrawn as to Claim 3 as amended.

Claim 4 stands rejected under 35 U.S.C. § 112, second paragraph. The Examiner states that in Claim 4, “the recitation of ‘a pulse width modulated drive signal from the output of the turn on delay circuit’ is indefinite because it is unclear as to if this pulse width modulated drive signal is the same as or is an additional signal to the output voltage of the turn on delay circuit recited in line 6.” (Office Action, page 2.) Applicants have therefore amended Claim 4 to recite “applying one of the pair of first pulse width modulated signals to a toggle circuit...” and “obtaining a second pulse width modulated drive signal from the output of the delayed turn-on circuit.”

Applicants respectfully submit that the foregoing amendment overcomes the rejection of the Examiner, and respectfully requests the 35 U.S.C. § 112, second paragraph, rejection be withdrawn as to Claim 4 as amended.

Claim 5 has been rejected under 35 U.S.C. § 112, second paragraph. The Examiner states that the recitation of “the modulated input control signals” in line 8 lacks proper antecedent basis. Applicants have therefore amended Claim 5 to recite, in the preamble, “A method of generating drive signals from a pair of pulse width modulated input control signals, comprising the steps of...”

Applicants respectfully submit that the foregoing amendment overcomes the rejection of the Examiner, and respectfully requests the 35 U.S.C. § 112, second paragraph, rejection be withdrawn as to Claim 5 as amended.

Claim 6 has been rejected under 35 U.S.C. § 112, second paragraph. The Examiner states that Claim 6, dependent upon Claim 5, is indefinite because of the technical deficiencies of Claim 5. (Office Action, page 2). Applicants have amended Claim 5, thereby rendering this rejection moot.

Applicants respectfully submit that the foregoing amendment of Claim 5 overcomes the rejection of the Examiner, and respectfully requests the 35 U.S.C. § 112, second paragraph, rejection be withdrawn as to Claim 6.

Claims 1-2 stand rejected under 35 U.S.C. § 102(b) as being unpatentable over U.S. Patent No. 4,015,213 to Hamada. Insofar as they may be applied against these claims, these rejections are respectively traversed.

Hamada is generally directed to obtaining a pulse width modulated ("PWM") output signal by comparing an input signal S_1 with an amplitude comparator and an internally generated sawtooth wave S_2 . The period of the PWM output is in part a function of a comparison value set at an amplitude comparator 14 compared to an attenuated signal S_1 . When the sawtooth wave S_2 reaches the amplitude of attenuated S_1 , a second pulse S_3 is generated. The pulse S_3 is used to toggle flip-flop circuit 15 in order to generate the PWM signal 6. A second signal S_4 is generated from the input signal S_1 . In Hamada, S_1 is summed in adder 2 to feedback from the amplified output of a D-class amplifier 5. This summed value is integrated and fed into an amplitude comparator 13, thereby generating signal S_5 . The negative pulse of S_5 substantially corresponds to the transition from an "on" part of the PWM duty cycle to the "off" part of the PWM duty cycle. (Figures 3 and 4A through 4E.)

Regarding Claim 1, the Examiner states that Hamada discloses "obtaining a constant width drive signal for the output (S_6) of the latch circuit" (Office Action, page 3.) Applicants respectfully disagree with the Examiner. In the present Application, "the circuits 10 and 14, of FIGURE 1, operate in the manner of set/reset latch circuits or of toggle circuits which are caused to change output levels with each positive transition of either one of input signals A and B to produce constant width (non-PWM) output drive signals." (Page 6, lines 22-26.) In contrast, the output S_6 of Hamada is width modulated. For example, in Figure 3 of Hamada, the output of the feedback circuit 8 is added to the summer 2, thereby potentially altering the duty cycle of the PWM. Furthermore, the input signal S_1 of Hamada can vary, thereby altering the amplified output S_6 , again modulating the output pulse width. This is not a "constant width drive signal from the output of said latch circuit." Applicants respectfully submit that the foregoing explanation traverses the rejection of the Examiner, and therefore respectfully request withdrawal of the rejection and allowance of Claim 1.

Claim 2 stands rejected under 35 U.S.C. § 102(b) as being unpatentable over Hamada. Claim 2 has been amended to more particularly recite a patentably distinguishing characteristic of the present invention, of "a toggle circuit ... whereby substantially symmetrical first and second output signals are generated from said toggle circuit." Support for this recitation is found in such places as both the preamble of Claim 2, and on page 7, lines 14-22.

Hamada does not disclose Claim 2 as amended. In Hamada, a substantially symmetrical output signal is not generated from the latch 15. Instead, as disclosed in Figure 4E, the time periods of T_1 and T_2 , the on and off duty cycle of the PWM, are substantially non-symmetrical. As detailed above, a non-symmetrical output can also be attributed to the input from the

feedback circuit 8, which affects the duty cycle of Hamada. Furthermore, a non-symmetrical output can also be attributed to a varying S_1 input signal. Applicants respectfully submit that the foregoing explanation and amendment of Claim 2 overcome the rejection of the Examiner, and therefore respectfully request withdrawal of the rejection and allowance of Claim 2.

In view of the foregoing, it is apparent that none of the cited references, either singularly or in any combination, teach, suggest, or render obvious the unique combination now recited in independent Claims 1 and 2. It is therefore submitted that Claims 1 and 2 clearly and precisely distinguish over the cited reference in a patentable sense, and are therefore allowable over this reference and the remaining references of record. Accordingly, it is respectfully requested that the rejection of Claims 1 and 2 under 35 U.S.C. § 102(b) as being unpatentable over Hamada be withdrawn.

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Applicants have now made an earnest attempt to place this application in condition for allowance. For the foregoing reasons and for other reasons clearly apparent, Applicants respectfully request full allowance of Claims 1 through 9.

Applicants do not believe any fees are due in connection with the filing of this paper; however, in the event that any fees are due, the Commissioner is hereby authorized to charge any required fees due (other than issue fees), and to credit any overpayment made, in connection with the filing of this paper to Deposit Account No. 50-0605 of the CARR LAW FIRM, L.L.P.

Should the Examiner have any questions or desire clarification of any sort, or deem that any further amendment is desirable to place this application in condition for allowance, the Examiner is invited to telephone the undersigned at the number listed below.

Respectfully submitted,

Date: _____

1/31/03



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AMENDMENT

VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the Claims:

1. (AMENDED) A method of creating a symmetrical [(constant width)] signal from a pair of pulse width modulated signals having equidistant start transition times, comprising the steps of:

applying one of the pair of pulse width modulated signals to a set input of a latch circuit;
applying the other of the pair of pulse width modulated signals to a reset input of the latch circuit; and
obtaining a constant width drive signal from the output of said latch circuit.

2. (AMENDED) Apparatus for generating a symmetrical (constant width) signal from a complementary pair of pulse width modulated signals having equidistant start and stop transition times, comprising:

a first pulse width modulated control signal supplying means;
a second pulse width modulated control signal supplying means;
a toggle circuit, connected to said first and second control signal supplying means, the toggle circuit supplying a first output drive signal level upon detecting a given characteristic of a first pulse width modulated control signal received from said first supplying means and supplying a second output drive signal level upon detecting said given characteristic of a second pulse width modulated control signal received from said second supplying means, whereby substantially symmetrical first and second output drive signals are generated from said toggle circuit.

3. (AMENDED) A method of generating a pulse width modulated signal and a symmetrical signal from a pair of pulse width modulated signals, comprising the steps of:

applying one of the pair of first pulse width modulated signals to a set input of a latch circuit as well as to a turn-on delay circuit wherein the turn-on delay is such that an output voltage transition of the turn-on delay circuit coincides with an output voltage transition of the latch circuit;

applying the other of the pair of first pulse width modulated signals to a reset input of the latch circuit;

obtaining a constant pulse width [(symmetrical)] drive signal from the output of said latch circuit; and

obtaining a second pulse width modulated drive signal from the output of the turn-on delay circuit.

4. (AMENDED) A method of generating a pulse width modulated signal and a symmetrical signal from a pair of pulse width modulated signals, comprising the steps of:

applying one of the pair of first pulse width modulated signals to a toggle circuit as well as to a delayed turn-on drive circuit wherein the turn-on delay is such that an output voltage transition of the delayed turn-on circuit coincides with an output voltage transition of the toggle circuit;

applying the other of the pair of first pulse width modulated signals to said toggle circuit;

obtaining a symmetrical drive signal from the output of said toggle circuit; and

obtaining a second pulse width modulated drive signal from the output of the delayed turn-on circuit.

5. (AMENDED) A method of generating drive signals from a pair of pulse width modulated input control signals, comprising the steps of:

applying both of a pair of pulse width modulated control signals to a first drive circuit;

toggling said first drive circuit between predetermined output drive signal voltage levels upon detection of a given transition characteristic of each of the pair of pulse width modulated input control signals; and

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delaying the application of one of said pair of pulse width modulated control signals to a second drive circuit whereby an output voltage transition of the second circuit coincides with an output voltage transition of the toggled drive circuit.